REMARKS

Prior to the present amendment and response, claims 1-20 were pending in the application. By this amendment, Applicant has amended the specification and has canceled claim 4. Thus, claims 1-3 and 5-20 remain in the present application. Reconsideration and allowance of pending claims 1-3 and 5-20 in light of the above amendments and the following remarks are respectfully requested.

A. Objections to the Drawings (Node 122 in Figure 1)

Applicant has carefully reviewed the Examiner's objections to the drawings. With respect to node SAIN 122 in Figure 1, Applicant points out that, as stated in the specification, this node would be coupled to an input of a sense amplifier. Thus, the nomenclature SAIN ("Sense Amp IN") is utilized. As the Examiner has pointed out, this node is in fact an output of cascode amplifier circuit 102. However, this output of cascode amplifier circuit 102 is used as an input of a sense amplifier. Applicant submits that Applicant can be its own lexicographer and label node 122 in view of its relation to the next stage, i.e. that this node is an input to a sense amplifier. This is also explained on, for example, page 7, line 18 through page 8, line 3 of the detailed description of the invention:

> "In Figure 1, cascode amplifier circuit 102 supplies bit line voltage ('DATAB') 120 to the drain of target memory cell 112 via bit line 116 during a read operation involving target memory cell 112, and generates sense amp input

voltage ('SAIN') 122 corresponding to target memory cell current 118 (also referred to as 'core cell current 118' and 'Icore 118') drawn by target memory cell 112 during the read operation. As discussed below, cascode amplifier circuit 102 provides higher DC gain at SAIN 122, resulting in significantly improved read operations involving target memory cell 112."

B. Objections to the Drawings (Depiction of FETs 104, 106, and 108)

Applicant has carefully reviewed the Examiner's objections to the drawings. With respect to depiction of FETs 104, 106, and 108 in Figure 1, Applicant points out that, these transistors are "intrinsic" NFETs with a Vt of approximately 0.3 to 0.5 volts as distinguished from FET 110 which is a "regular" NFET with a Vt of approximately 0.7 to 1.0 volts. See, for example, page 8, line 20 to page 9, line 1 of the detailed description of the invention. As such, Applicant has appropriately used two different symbols to distinguish these two different types of NFETs. To designate PFETs, such as PFETs 124 and 126, Applicant has used a third symbol distinct from the other two symbols. It is noted that, since the detailed description has appropriately defined the different symbols, there would be no confusion regarding the use of the small circles on the gates of FETs 104, 106, and 108. Accordingly, Applicant submits that it can be its own lexicographer, and it is respectfully requested that the Examiner's objections to the drawings be removed.

C. **Rejections of Claims 1-20 Under 35 USC § 112, ¶2**

The Examiner has rejected claims 1-20 under 35 USC § 112, ¶ 2 stating that the term "intrinsic FET" has not been defined in the application. However, as stated above, "intrinsic" NFETs have been defined in the present application as those NFETs with a Vt of approximately 0.3 to 0.5 volts as distinguished from "regular" NFETs with a Vt of approximately 0.7 to 1.0 volts. See, for example, page 8, line 20 to page 9, line 1 of the detailed description of the invention.

The Examiner has further rejected claims 1-20 under 35 USC § 112, ¶ 2, requesting a clarification regarding "target memory cell and bit line." As requested by the Examiner, Applicant clarifies that, as the Examiner has suggested, the "target memory cell and bit line" are not part of the claimed invention, and claim 6 is not intended to affect the fact that the "target memory cell and bit line" are not part of the claimed invention.

D. **Conclusion**

For the foregoing reasons, Applicant respectfully submits that claims 1-3 and 5-20 are in condition for allowance and an early notice of allowance directed to claims 1-3 and 5-20 remaining in the present application is respectfully requested.

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Respectfully Submitted,
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